



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

GB1

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|-----------------|-------------|----------------------|---------------------|
|-----------------|-------------|----------------------|---------------------|

09/170,336 10/13/98 BEETESON

J UK9-98-026

WM02/0925

IBM CORP
IP LAW DEPT
TJ WATSON RESEARCH CENTER
P O BOX 218
YORKTOWN HEIGHTS NY 10598

EXAMINER

NGUYEN, K

ART UNIT

PAPER NUMBER

2674

12

DATE MAILED:

09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

SM

Office Action Summary

Application No.

09/170,336

Applicant(s)

BEETESON ET AL.

Examiner

Kevin M. Nguyen

Art Unit

2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 July 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

The amendment filed on 7/9/2001 is entered. The rejections of claims 1-11 are maintained.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (U.S. Patent No. 5,818,403).**

3. As to claim 1, Nakamura et al teaches a matrix addressed display device (see col. 7, lines 10-13), which includes a cathode means (see col. 7, line 30). Figure 3 shows grid electrode means lines X1, X2, ... having a plurality of electron-emitting and modulation electrodes Y1, Y2, ... are arranged to form an XY matrix corresponding to the claimed grid electrode means (see col. 5, lines 25-29), with this apparatus, at a voltage of from 5 to 10 kV applied to the transparent electrode 66, cut-off control was practicable at a voltage of the modulation electrode 64 of -30 V or more negative voltage (see col. 9, lines 8-11), the information signals for the scanning line of M=1, information signals to be inputted to even-numbered modulation electrodes (N=2, 4,...) are stored in a memory 80, while the information signals to be inputted to odd-numbered modulation electrodes (N=1, 3, 5,...) are inputted directly thereto by a voltage application means 81 as modulation voltages (V_{m1} , V_{m3} , V_{m5} ,...) including ON

voltages, cut-off voltages and gradation voltages in corresponding with the information signals. During this period, a cut-off voltage (V_{off}) is applied to the even-numbered modulation electrodes ($N=2, 4, \dots$) irrespective of the information signals according to cut-off the signals sent out from the signal switching circuit (signal separation means) 82 to a voltage application means 83 (col. 9, lines 28-41). It would have been obvious to a person of ordinary skill in the art to recognize that Nakamura discloses means for providing cut-off correction information to a one of the first or the second plurality of parallel conductors as claimed.

4. As to claim 2, Nakamura et al teaches a voltage application means 81 (Amp) as modulation voltage ($V_{m1}, V_{m3}, V_{m5}, \dots$) corresponding to the claimed means for providing gain correction information (fig.13, col. 9, lines 33-34).

5. As to claims 3-11, Nakamura et al teaches the information signals for the scanning line of $M=1$, information signals to be inputted to even-numbered modulation electrodes ($N=2, 4, \dots$) are stored in a memory 80 (col. 9, lines 28-31). It would have been obvious to a person of ordinary skill in the art to recognize that Nakamura discloses a non-volatile memory for storing a plurality of values for cut-off and gain correction information as claimed.

6. **Claims 1-11 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (Europe Patent No. 0,688,035) (IDS).**

7. As to claim 1, Suzuki teaches a flat cathode display device 101 which includes the correction-data creating circuit 4114 creates correction data by calculating the electron emission efficiency of the each element based upon monitoring of the currents

is and i.e. sensed for each elements (see Fig. 22, page 23, lines 35-37). It would have been obvious to a person of ordinary skill in the art to recognize that Suzuki discloses means for providing cut-off correction information to a one of the first or the second plurality of parallel conductors as claimed (by virtue of the operation described at page 23, line 38 to page 24, line 31).

8. As to claim 2, Suzuki teaches as illustrate in Fig. 44B, an operational amplifier 2601 (see page 29, lines 27-33), the correction circuit 7489 (see Fig. 42, page 29, lines 34-37). It would have been obvious to a person of ordinary skill in the art to recognize that Suzuki discloses means for providing gain correction information to a one of the first and second plurality of parallel conductors as claimed.

9. As to claims 3-11, Suzuki teaches a random-access memory (see page 18, line 41). It would have been obvious to a person of ordinary skill in the art to recognize that Suzuki discloses a non-volatile memory for storing a plurality of values for the cut-off and gain correction information as claimed.

Response to Arguments

10. Applicant's arguments filed 1/30/2001 have been fully considered but they are not persuasive.

11. In response to applicant's argument that claim 1 recites "cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonal to the row conductors; means for providing cut-off correction information to a one of the first or second plurality

of parallel conductors." Claim 2 recites "means for providing gain correction information to a one of the first or the second plurality of parallel conductors."

This argument is not persuasive because Nakamura's invention teaches "a matrix addressed display device (col. 7, lines 10-13) which includes a cathode means (col. 7, line 30), a voltage application means 81 as modulation voltages (V_{m1} , V_{m3} , V_{m5} ...) including ON voltages, cut-off voltages and gradation voltages in corresponding with the information signals. During this period, a cut-off voltage (V_{off}) is applied to the even-numbered modulation electrodes ($N=2, 4...$) irrespectively of the information signals according to cut-off the signals sent out from the signal switching circuit (signal separation means) 82 to a voltage application means 83 (col. 9, lines 28-41)." These argument are not persuasive because it would have been obvious to a person of ordinary skill in the art to recognize that Nakamura discloses the cut-off signal / gain information circuit 81 and 83 which are the equivalent circuit to cut-off correction information and gain correction information as claimed.

This argument is not persuasive because Suzuki's invention also teaches "a flat cathode display device 101 which includes the correction-data creating circuit 4114 creates correction data by calculating the electron emission efficiency of the each element based upon monitoring of the currents is and I.e. sensed for each elements (see Fig. 22, page 23, lines 35-37), as illustrate in Fig. 44B, an operational amplifier 2601 (see page 29, lines 27-33), the correction circuit 7489 (see Fig. 42, page 29, lines 34-37)." These arguments are not persuasive because it would have been obvious to a person of ordinary skill in the art to recognize that Suzuki discloses means for providing

cut-off correction information to a one of the first or the second plurality of parallel conductors; and means for providing gain correction information to a one of the first and second plurality of parallel conductors as claimed.

For these reasons, the rejections of claims 1-11 based on Nakamura et al and Suzuki et al have been maintained.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on M-F (9:00-5:00), with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

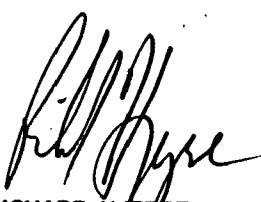
(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

KN
September 18, 2001


RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600